Remarks

In the Office Action mailed June 2, 2004, the Examiner rejected claims 1-5 and 7-11, and indicated allowance of claim 6, if rewritten in independent form. The Applicants thank the Examiner for the indication of allowable material and the detailed references provided, but respectfully traverse the rejection of claims 1-5 and 7-11.

Regarding Amendments to the Specification

The Examiner objected to the specification as written as "lacking an enabling description for claim 7." (Office Action at 2). Applicants traverse this objection. However, the specification have been amended as required by the Examiner. The specification was reworded to more clearly set forth the mathematical expression of the disclosed equation.

Regarding Amendment of Claims

The Examiner objected to claims 1-11 due to informalities. (Office Action at 2). In addition, the Examiner required indentation within the claim language to segregate subcombinations or related steps. (Office Action at 2). The required indentations have been made, without changing the scope of the claims, and to conform to 37 C.F.R. § 1.75 and MPEP § 608.01(m), as required by the Examiner.

Regarding Rejection of Claims under 35 U.S.C. § 112

The Examiner rejected claim 1-10 under 35 U.S.C. § 112 as failing to comply with the enablement requirement.

Regarding the rejection of claim 7 as failing to comply with the enablement requirement, the Applicants have addressed this requirement of the Examiner, as noted previously.

Regarding the rejection of claims 1-10, the Examiner objected to the use of indefinite language and for failing to point out and distinctly claim the subject matter which the Applicants regard as the invention. (Office Action at 3). The Applicants addressed the language as required by the Examiner.

Regarding Rejection of Claims under 103(a)

The Examiner rejected claims 1-5 and 7-11 under 35 U.S.C. § 103(a) over Hashimoto (U.S. No. Patent 6,263,43). Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, three basic criteria must be satisfied. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine references. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all of the claim elements. See M.P.E.P. § 2143. Moreover, the requisite teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Applicant's disclosure. *See In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). *See* M.P.E.P. § 706.02(j).

A *prima facie* case of obviousness has not been established because, among other things, Hashimoto does not teach or suggest every element of claims 1-5 or 7-11.

Regarding Claims 1 and 3:

Claims 1 and 3 each recite:

> supplying a test input signal to a semiconductor device as a testing target and receiving an output signal from the semiconductor device . . . detecting an optimal value of the wait time," and "measuring, after elapse of the wait time, the electrical characteristics of the semiconductor device on the basis of the response signal outputted from the semiconductor device . . . making an OK/NG decision on the electrical characteristics of the semiconductor device on the basis of the measurement results . . . if the decision is "NG", remeasuring the electrical characteristics under a newly set wait time," and "performing the remeasuring operation on the electrical characteristics until the result of a decision is "OK."

In contrast, in Hashimoto, wait time, which is the time when test signals are supplied to the semiconductor device until signals output from the semiconductor device are measured, are not optimized. Further, Hashimoto does not "explicitly disclose detecting an optimal value of the wait time," as stated by the Examiner in direct contradiction of the Examiner's earlier statement that Hashimoto "substantially discloses a . . . [d]etecting an optimal value of the wait time." (Office Action at 5 and 4).

Further, regarding independent claims 1, 3, 9 and 10, the Examiner asserts that "it would have been obvious to a person having ordinary skill in the art . . . to perform timing adjustments of the output response signals from the semiconductor device DUT. . . [and] to determine whether the semiconductor device works correctly or not," (Office Action, page 6). Applicants disagree with this assertion. The Examiner has made a conclusive statement which the prior art does not teach, motivate or suggest. If taking Official Notice, Applicants request that the Examiner cite references in support of the Examiner's assertion or provide an affidavit if it is within the Examiner's personal knowledge as required by MPEP § 2144.03.

Therefore, Hashimoto does not disclose each and every element of claims 1 and 3. For at least this reason, claims 1 and 3 should be allowed.

Regarding Claims 5 and 11:

Claim 5 recites "a measuring device for setting a test measuring condition," and "performing the measurement on the semiconductor device under the set test measuring condition." Claim 5 further recites, "a measurement control apparatus for deciding a stable state of the output signal of the semiconductor device," then "counting the number of measurements . . . analyzing in realtime," the measurements and "deciding a stable state." Similarly, claim 11 recites "deciding a state of the measured data from the result of analysis" and "deciding whether or not the number of measurements . . . has reached the calculation target number."

Hashimoto does not disclose a method for performing counting and analyzing, in realtime, measurements to establishing a stable state of a measurement. Moreover, the Examiner has stated that Hashimoto does not "explicitly disclose a measuring loop for performing measurements in a repeated way . . . for automatically detecting the optimal wait time value." (Office Action at 6). Therefore, Hashimoto does not disclose at least this element, and does not disclose each and every element of claims 5 and 11.

In support of the rejection under 35 U.S.C. § 103, the Examiner contends that the findings of *In re Aller* apply to Hashimoto with regard to the present application and states that it is "not inventive to discover the optimum or workable ranges by routine experiment, such as in this case performing measurements on a semiconductor device in a repeatable way for obtaining an optimal value." (Office Action at 7).

Applicants disagree and rebut that in *In re Aller*, 105 U.S.P.Q. 233 (C.C.P.A. 1955), is not appropriate in this situation. In *In re Aller*, the court presumes that the concentration and temperature in an organic synthesis context can be optimized without undue experimentation, and this presumption applied only to concentration and temperature ranges in the organic chemistry arts in which *In re Aller* was interested. The Examiner has not cited any evidence, scientific or legal, to show that any such presumption exists in the electrical or materials arts regarding Applicants' claimed methods. Further, *In re Aller* does not state that a method of optimizing a method of testing, as in the present application, is the equivalent of discoveries based on routine experiment. Therefore, Applicants contend that the application of *In re Aller* here is not appropriate, given the limited scope of the cited decision.

For at least these reasons, that Hashimoto does not disclose each and every element of claims 5 and 11, and the application of *In re Aller* is not appropriate, claims 5 and 11 are allowable.

Regarding Claims 9 and 10:

Claim 9 and 10 each recite "supplying a test signal to the semiconductor device and, upon receipt of a response signal outputted from the semiconductor device in accordance with the test signal after an elapse of the initialized wait time," and "effecting an OK/NG decision . . . in accordance with the result of measurement."

As per the above discussion, the Examiner recognized that Hashimoto does not "does not explicitly disclose a measuring processing loop for performing measurements in a repeated way." (Office Action at 6). The Examiner contends, in support of the rejection under 35 U.S.C. § 103, "it would have been obvious to a person having ordinary skill in the art . . . so as to ensure

the proper operation of a semiconductor device under test." (Office Action at 7). Applicants disagree with this assertion. The Examiner's statement provided no support that Hashimoto discloses the missing element of the present application, i.e. the measuring processing loop, as noted by the Examiner, nor does the Examiner provide support that Hashimoto suggests, teaches, or motivates "effecting of an OK/NG decision" as stated in claims 9 and 10. Applicants respectfully request that the Examiner withdrawal the rejection under 35 U.S.C. § 103, or cite references in support of the Examiner's assertion, or provide an affidavit if it is within the Examiner's personal knowledge as required by MPEP § 2144.03.

For at least the reasons above, Hashimoto does not disclose each and every element of claims 9 and 10 and should be allowed. Therefore, claims 9 and 10 are allowable.

Regarding claims 1-11:

The present application discloses an apparatus and method for optimizing wait time until an output signal from the semiconductor device is stabilized. Measurement of electrical characteristics of the semiconductor device is carried out by measuring, and after test signals are supplied, signals are output from the semiconductor device after the optimized wait time.

As recited in claims 1-4, 9 and 10, test signals are supplied to the semiconductor device, an OK/NG decision on the electrical characteristics of the semiconductor device after a predetermined wait time is made, and wait time is adjusted based on the result of the decision. Furthermore, as recited in claims 5-8 and 11, the electrical characteristics of the semiconductor device are measured for a plurality of times, the stability of the measured data is decided based on the measurement result obtained from the measurement, and if the data is decided to be stable, optimal value of the wait time is calculated from a plurality of real measurement times.

In contrast, in Hashimoto (US 6,263,463), wait time, which is the time since test signals are supplied to the semiconductor device until the signals output from the semiconductor device are measured, are not adjusted. That is, in Hashimoto, the time of input of the signals supplied to the DUT is adjusted based on the output signals from the DUT.

Conclusion:

For the reasons set forth above, Applicants respectfully submit that the rejection under 35 U.S.C. § 103 should be withdrawn and that independent claims 1, 3, 5, and 9-11 should be allowed. In addition, since claims 2, 4, and 6-8 are respectively dependent claims from claims 1, 3, and 5, dependent claims 2, 4, and 6-8 should be allowed for at least the same reasons as set forth with respect to claims 1, 3 and 5.

Therefore, Applicants respectfully request reconsideration by the Examiner of all claims and timely allowance of claims 1-11.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: October 8, 2004

By: Richard V. Burgujian
J. Robert Chromcak, Jr. #27,432
Richard V. Burgujian
Reg. No. 31,744